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METHOD FOR COMPARING THE ADDRESS OF A MEMORY ACCESS WITH AN ALREADY KNOWN ADDRESS OF A FAULTY MEMORY CELL

Cross-Reference to Related Application:

This application is a continuation of copending International Application No. PCT/EP02/03913, filed April 9, 2002, which designated the United States and which was not published in English.

Background of the Invention:

Field of the Invention:

The invention lies in the memory technology field. More specifically, the invention relates to a method for comparing the address of a memory cell with an already known address of a faulty memory cell in a semiconductor memory module which is subdivided into banks and has an address structure in which each address is associated with a bank which is organized in rows and columns and is defined by way of a row address, a column address, and a bank address.

Until now, essentially only the rows - or alternatively the column address - have been compared with the faulty address in the method under discussion. As soon as an address hit is achieved, the method provides for the entire row or the

entire column to be replaced by a replacement row or replacement column. The primary problem with the previous method is that the comparison between the addresses does not take place sufficiently quickly, so that, in particular, real-time comparison is impossible. The conventional method wastes redundant memory space by globally replacing entire rows or entire columns when an address hit is found.

A method for comparing the entire address of an access and of an already-known address of an individual faulty memory cell is known from an article by Lucente, Harris, and Muir: *Memory system reliability improvement through associative cache redundancy*, in: IEEE J. of Solid-State Circuits, Vol. 26, No. 3, March 1991, pages 404-09.

Summary of the Invention:

It is accordingly an object of the invention to provide a method for comparing a memory access address with a known address of a faulty memory cell which overcomes the above-mentioned disadvantages of the heretofore-known devices and methods of this general type and which method can be carried out sufficiently quickly so that real-time determination is possible, and which does not lead to memory space being wasted.

Since, in the case of the method according to the invention, not only the row addresses but also the column addresses and bank addresses are always determined when a memory access takes place, this avoids redundant memory space being wasted since this specific determination of fault locations in the memory also means that replacements are required only for these specific addresses in the address structure.

One particularly advantageous embodiment of the method according to the invention, which guarantees real-time processing owing to the use of a process whose timing has been tightened up for address determination, provides for the row address as well as the column address and the bank address to be determined as follows:

in a first cycle, one row is activated using a row address and the associated bank address,

in a second cycle, the activated row is accessed using a column address and a bank address,

during the activation of the row:

a) the row address of the activated row is compared with the row address of the faulty memory cell, and the comparison result is passed to a latching circuit whose output signal is passed to a logic stage,

b) the column address is compared with the column address of the faulty memory cell and the comparison result is passed to the logic stage,

c) the bank address is compared with the bank address of the faulty memory cell and the comparison result is passed to the logic stage,

d) an activation pulse is obtained from the rising flank of the bank selection signal in a pulse generator and is passed to the latching circuit if the comparison of the bank address with the bank address of the faulty memory cell produces a match and an enable register (EN) is set,

e) the latching circuit outputs a latching signal if the comparison result in step a) is positive and an activation pulse (ACTP1) has arrived from step d), and

the logic stage outputs a hit signal, which indicates access to a faulty memory cell, if the comparison results in steps b) and c) are positive and the latching circuit is outputting the latching signal.

The invention also achieves the following advantages: some of the comparison steps are actually carried out in an early comparison stage while some of the other comparison processes, those which take place in the second time-critical

cycle, are reduced in number due to the use of a latching circuit. Furthermore, determination reliability is provided in that the latching circuit always automatically contains the correct value whenever a determination process is activated.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a method for comparing the address of a memory access with an already known address of a faulty memory cell, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawing.

Brief Description of the Drawing:

The single figure of the drawing is a schematic of a part of a semiconductor module that is configured according to the invention.

Description of the Preferred Embodiments:

Referring now to the figure of the drawing in detail, there is shown a pulse generator 10. Three comparison stages 11, 12, and 13 provided. Two logic stages 14 and 15 are suitable connected to the comparison stages. A latching circuit or a latch is annotated by the reference number 16, and a logic stage is shown at 17. A reference number 18 refers to a faulty bank address (BA_fail). A faulty row address is annotated by the reference number 19 (RA-fail). A faulty column address is annotated by the reference number 20 (CA_fail), and a register set (EN) is annotated by the reference number 21.

The elements mentioned above are connected or linked to one another as follows: the faulty bank address 18 is passed to one input of the comparison stage 11. A bank address is applied to the other input of this comparison stage 11. The faulty row address 19 is applied to one input of the comparison stage 12. A row address RA is applied to the other input of the comparison stage 12. The faulty column address 20 is applied to one input of the comparison stage 13. The

column address CA is applied to the other input of the comparison stage 13.

The output of the logic stage 11 is applied to one input of the logic stage 14. The register set 21 is applied to the other input of the logic stage 14. The output of the comparison stage 14 is applied to one input of the logic stage 15. The output signal from the pulse generator 10 is applied to the other input of the logic stage 15. One or more bank selection signals (BNKSEL) is or are applied to the input of the pulse generator 10.

The output signal from the logic stage 15 is applied to one input of the latching circuit 16. The output of the comparison stage 12 is applied to the other input of the latching circuit 16. The logic stage 17 has three inputs, to one of which the output signal of the latching circuit 16 is applied, while the output signal from the comparison stage 11 is applied to a second input. The output from the comparison stage 13 is applied to the third input of the logic stage 17. The circuit explained above operates as follows:

When a memory access occurs, one row is activated in a first cycle, using a row address RA and the associated bank address BA. In the next, second cycle, the activated row is accessed using a bank address BA and a column address CA. By way of

example, four independent banks may be provided. A maximum of one row may be activated in each bank. The number of banks depends on the architecture and may differ from the stated number 4. However, this changes nothing relating to the basic principle of the operation of the banks.

A pulse ACTP (Activation Pulse) is derived in the pulse generator from the rising flank of the bank selection signal (BNKSEL) during the row activation in the first cycle mentioned above. At the same time, the bank address BA which is being used at that time is compared with the known faulty bank address 18 (BA_fail). If these two addresses match and if the entire register set 21 (EN) is active (EN = 1), the ACTP pulse is passed to the latching circuit 16 in the form of a pulse ACTP1. Using the pulse ACTP1 which has been passed to it, the result of the comparison of the current row address RA with the known faulty row address 19 (RA_fail) is locked or latched in the latching circuit 16. If the row addresses match, the output from the latching circuit 16 produces a logic 1. All this takes place during a single clock cycle which, in the end, ensures real-time address comparison. A relatively long time is available for this comparison since the actual access to data cannot take place, at the earliest, until the next cycle.

During the column access, the current column address CA must now also be compared with the known faulty column address 20 (CA_fail). Furthermore, the current bank address BA must be compared with the already known faulty bank address 18 (BA_fail). If the result of the two comparisons is positive and/or they produce a match, and if the latching circuit 16 is set from the comparison previously referred to, the output of the logic stage 17 changes to hit or logic 1, thus signaling access to a defective memory cell.

The method mentioned above has the advantage that an entire sequence of the necessary comparison accesses actually takes place at an early stage in the method, during which sufficient time is available for this purpose. Furthermore, the number of comparisons in the previously mentioned second, time-critical cycle is greatly reduced. Finally, the latching circuit automatically always contains the correct value whenever it is activated.